

EAST - [10605590.wsp:1]

File View Edit Tools Window Help

Drafts
Pending
Active
L2: (78288) DRAM\$1 or dynamic adj rand
L3: (12) 2 and (bitline near contact\$1 and
L5: (1) 4 and (bitline near contact\$1)
L6: (1) 4 and (bitline and contact)
L7: (1) 4 and (bitline)
L4: (72) 2 and ((memory near cell) and (e
L8: (515) 2 and (bitline near contact\$1 and
L9: (1104) 2 and (bitline and contact\$1 and
L10: (1) 9 and ((memory near cell) and (e
L11: (346) 9 and ((memory near cell\$1) ai
L12: (120) 11 and (bitline near contact\$1)
L13: (111) 12 and (conduct\$3 and periphe
L14: (115) 12 and (bitline adj contact\$1)
Failed
(0) 2 and (bitline near contact\$1 and (trou
Saved
(71397) DRAM\$1 or dynamic adj random
(1) (DRAM\$1 or dynamic adj random adj
(12) (DRAM\$1 or dynamic adj random adj
Favorites
Tagged (0)
UDC
Queue
Trash

DBs: USPAT:EPO:JPO:DERWENT:IBM:TDB
Default operator: GR
Plurals
Highlight all hit terms initially

12 and (bitline adj contact\$1)

ABST I56F Image Text HTML

	U	I	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
1	<input type="checkbox"/>	<input type="checkbox"/>	US 6750494 B1	20040615	10	Semiconductor buried contact with a removable spacer	257/296	257/202; 257/390
2	<input type="checkbox"/>	<input type="checkbox"/>	US 6735132 B2	20040511	11	6F2 DRAM array with apparatus for stress testing an isolation gate and method	365/201	365/190; 365/200
3	<input type="checkbox"/>	<input type="checkbox"/>	US 6727539 B2	20040427	17	Embedded vertical DRAM arrays with silicided bitline and polysilicon interconnect	257/296	257/288
4	<input type="checkbox"/>	<input type="checkbox"/>	US 6727538 B2	20040427	13	Method and structure for improved alignment tolerance in multiple, singularized	257/296	257/306; 257/774
5	<input type="checkbox"/>	<input type="checkbox"/>	US 6723623 B1	20040420	15	Methods of forming implant regions relative to transistor gates	438/525	438/142; 438/279
6	<input type="checkbox"/>	<input type="checkbox"/>	US 6713340 B2	20040330	61	Method for fabricating a memory device	438/239	438/381
7	<input type="checkbox"/>	<input type="checkbox"/>	US 6710391 B2	20040323	32	Integrated DRAM process/structure using contact pillars	257/306	257/295; 257/310
8	<input type="checkbox"/>	<input type="checkbox"/>	US 6693041 B2	20040217	18	Self-aligned STI for narrow trenches	438/702	438/723
9	<input type="checkbox"/>	<input type="checkbox"/>	US 6687146 B2	20040203	17	Interleaved wordline architecture	365/63	365/149; 365/190
10	<input type="checkbox"/>	<input type="checkbox"/>	US 6686633 B1	20040203	26	Semiconductor device, memory cell, and processes for forming them	257/392	257/396; 257/403
11	<input type="checkbox"/>	<input type="checkbox"/>	US 6667223 B2	20031223	9	High aspect ratio high density plasma (HDP) oxide gapfill method in a lines and	438/427	257/E21.548; 438/435